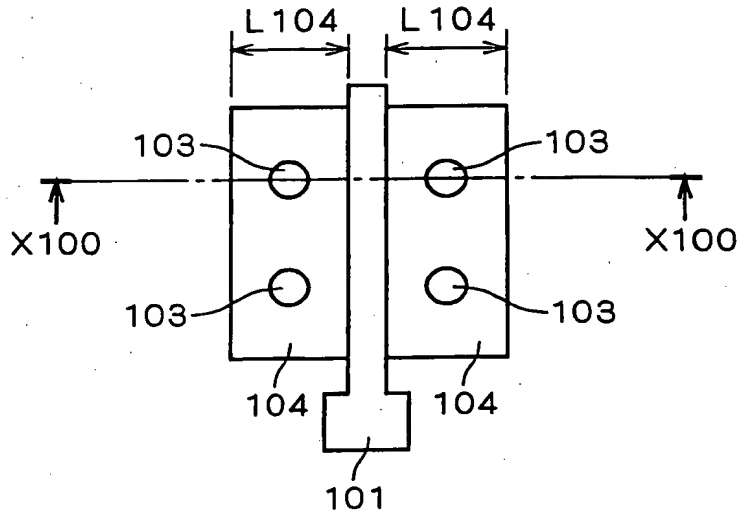


This cross-sectional view shows a semiconductor device with a central opening 101. The device is built on a substrate 106, which is covered by a layer 107. A layer 108 is formed on top of 107, and a layer 109 is formed on top of 108. The central opening 101 is defined by a wall 110. The opening is filled with a material 114, and a layer 115 is formed on top of 114. The opening is surrounded by a layer 113. The opening is also surrounded by a layer 116, which is formed on top of 113. The opening is also surrounded by a layer 117, which is formed on top of 116. The opening is also surrounded by a layer 119, which is formed on top of 117. The opening is also surrounded by a layer 118, which is formed on top of 119. The opening is also surrounded by a layer 111, which is formed on top of 118. The opening is also surrounded by a layer 112, which is formed on top of 111. The opening is also surrounded by a layer 104, which is formed on top of 112. The opening is also surrounded by a layer 103, which is formed on top of 104. The opening is also surrounded by a layer 105, which is formed on top of 103. The opening is also surrounded by a layer 102, which is formed on top of 105. The opening is also surrounded by a layer 101, which is formed on top of 102.

Figure 1 is a schematic diagram of a device 100. The device includes a central vertical member 101. Two rectangular blocks 102 are positioned on either side of the upper portion of member 101. Each block 102 contains two circular features 103. The horizontal distance from the central axis of member 101 to the center of each circular feature 103 is indicated by the dimension L102.



**FIG. 28 BACKGROUND ART**



**FIG. 29 BACKGROUND ART**

